Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **14EC2070** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ASIC DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Compare the features of different types of ASICs with neat diagrams. | CO3 | 15 |
| b. | Sketch the ASIC design flow. | CO1 | 5 |
| (OR) | | | | |
| 2. | a. | Demonstrate the structure and operation of Poly–diffusion antifuse and Metal–Metal Antifuse. | CO3 | 8 |
| b. | Sketch a four-input NOR gate and calculate its logical effort . | CO3 | 6 |
| c. | Apply CMOS Logic to implement the given function.  F = (A+B+C) (D+E) | CO3 | 6 |
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| 3. |  | Demonstrate the Altera MAX architecture and its timing model with necessary diagrams. | CO2 | 20 |
| (OR) | | | | |
| 4. | a. | With block diagram of XC4000 CLB and describe its function. | CO2 | 15 |
| b. | Implement the given function in PAL structure of an Altera device.  F = A' · C · D + B' · C · D + A · B + B · C' | CO2 | 5 |
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| 5. | a. | Brief about hierarchical nature of an EDIF file. | CO3 | 5 |
| b. | Describe the EDIF file for an inverter icon. | CO3 | 15 |
| (OR) | | | | |
| 6. | a. | Illustrate the interconnect architecture used in an Actel ACT family FPGA with neat diagrams. | CO2 | 15 |
| b. | Analyze delay in Actel interconnect using Elmore delay method. | CO2 | 5 |
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| 7. | a. | Define floorplanning in ASIC Design? Point-out the goals and objectives of floorplanning. | CO1 | 5 |
| b. | Analyze routing congestion in floorplanning. | CO1 | 7 |
| c. | Demonstrate Channel definition and ordering in floorplanning with examples. | CO1 | 8 |
| (OR) | | | | |
| 8. | a. | Define placement in ASIC Design? Point-out the goals and objectives of placement. | CO1 | 5 |
| b. | Illustrate different Iterative Placement Improvement methods with diagrams. | CO1 | 15 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Point-out the goals and objectives of global routing and detailed routing. | CO1 | 6 |
| b. | Demonstrate Global Routing between blocks and Inside Flexible Blocks. | CO1 | 14 |